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DOCKET NO. 04-SH-122 **PATENT**
CLIENT NO. STMI01-04122
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Stuart Ryan, et al.
Serial No.:	10/621,012
Filed:	July 15, 2003
Title:	PROTOTYPING INTEGRATED SYSTEMS
Art Unit No.:	2185
Examiner:	Denise Tran

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

The undersigned hereby certifies that the following documents:

1) Response to Notice of Non-Compliant Appeal Brief;
2) Substitute Appeal Brief; and
3) Postcard receipt

relating to the above application, were deposited as First Class Mail, with the United States Postal Service, addressed to MAIL STOP APPEAL BRIEF-PATENTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 1/26/07.

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RESPONSE TO NOTICE OF NON-COMPLIANT APPEAL BRIEF

In response to the Notice of Non-Compliant Appeal Brief dated January 17, 2007, the Applicant is submitting a Substitute Appeal Brief.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *dvenglarik@munckbutrus.com*.

The Commissioner is hereby authorized to charge any fees connected with this

communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS, P.C.

Date: 1-26-2007

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SUBSTITUTE APPEAL BRIEF

This Substitute Brief is submitted on behalf of Appellant for the application identified above.

Please charge any additional necessary fees to Deposit Account No. 50-0208.

REAL PARTY IN INTEREST

The real party in interest for this appeal is the assignee of the application, STMICRO-ELECTRONICS, INC.

RELATED APPEALS AND INTERFERENCES

None – there are no appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this pending appeal.

STATUS OF CLAIMS

Claims 1–26 are pending in the present application. Claims 1–6, 8–9, 12–17 and 20–26 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,907,514 to *Mitsuishi*. Claims 7, 10–11 and 18–19 are objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims. The rejection of claims 1–6, 8–9, 12–17 and 26 is appealed.

STATUS OF AMENDMENTS

No amendment to the claims was filed following the final Office Action mailed February 28, 2006.

SUMMARY OF CLAIMED SUBJECT MATTER

The following summary refers to disclosed embodiments and their advantages but does not delimit any of the claimed inventions.

In General:

The present application is directed, in general, to prototyping integrated systems. When prototyping integrated systems comprising a processor and memory, it is useful to test the design with the processor fabricated in an integrated circuit and the memory resources provided or emulated off-chip and accessed either through bonding-out the processor or through existing off-chip communication ports. Specification, page 1. However, bonding-out the processor to make its signals available off-chip uses many pins, requires to the processor to run at reduced speed so that the off-chip interface functions reliably, and constrains testing for designs where some resources are integrated while others are not. Specification, page 1. Using existing communication ports can require software assistance to enable the port to function, creating a difference between the prototype and final designs, and may require a different address map from final design. Specification, pages 1–2.

Support for Independent Claims:

Per 37 C.F.R. § 41.37, only support for the independent claims is discussed herein. The discussion of the claims in this section is for illustrative purposes and is not intended to affect the scope of the claims.

In the embodiment to which independent claim 1 is directed, an integrated system 2 includes a processor 6 that issues memory access requests and at least one on-chip resource, Resource 1 10 and/or Resource 2 12:

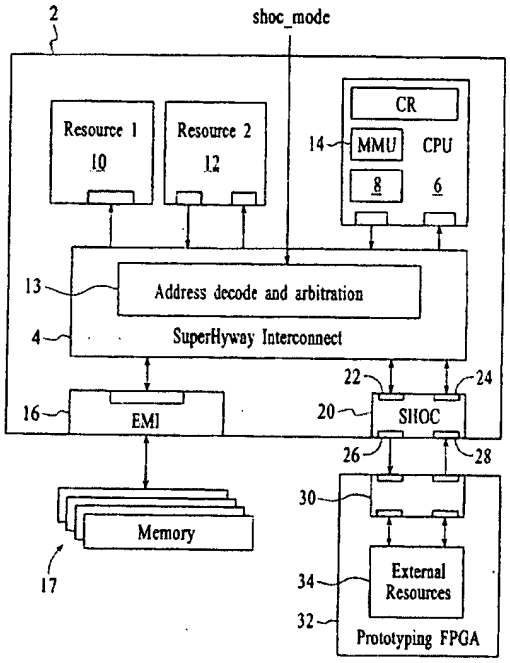


FIG. 1

Specification, Figure 1, page 4. The memory access requests identify an address addr. in memory 17 to which the request is directed:

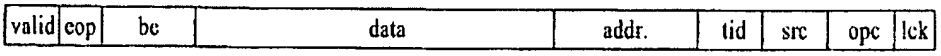


FIG. 2

Specification, Figure 2, page 5. Packets containing memory access requests and addressable within

the address space of the processor may be directed off-chip through a SuperHyway off-chip (SHOC) interface 20 or equivalently through an external memory interface (EMI) 16. Specification, page 4.

Two address maps are employed by integrated system 2, a first address map (Figure 3) and a second address map (Figure 4):

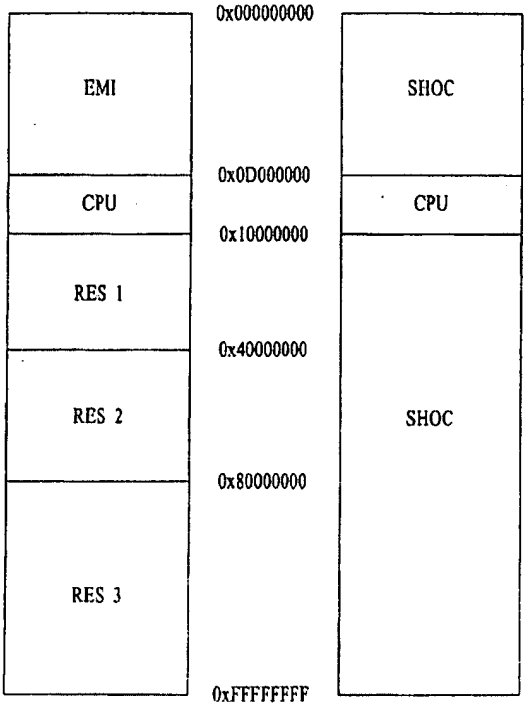


FIG. 3 FIG. 4

Specification, Figures 3–4, pages 6–7. The first address map has a range of addresses 0x10000000 to 0x3FFFFFFF allocated to the at least one on-chip resource Resource 1 ("RES 1") 10 and a second range of addresses 0x00000000 to 0x0CFFFFFF allocated to the SHOC interface 20/external memory interface 16, while the second address map has the first range of addresses also mapped to

the SHOC interface 20. Specification, Figures 3–4, pages 6–7. Decode logic ("request directing unit") within SuperHyway Interconnect router 4 includes the two address maps 48 and 50 and selects one based on a mode signal shoc_mode 46 to direct memory access requests to either the on-chip resource Resource 1 or the SHOC interface 20:

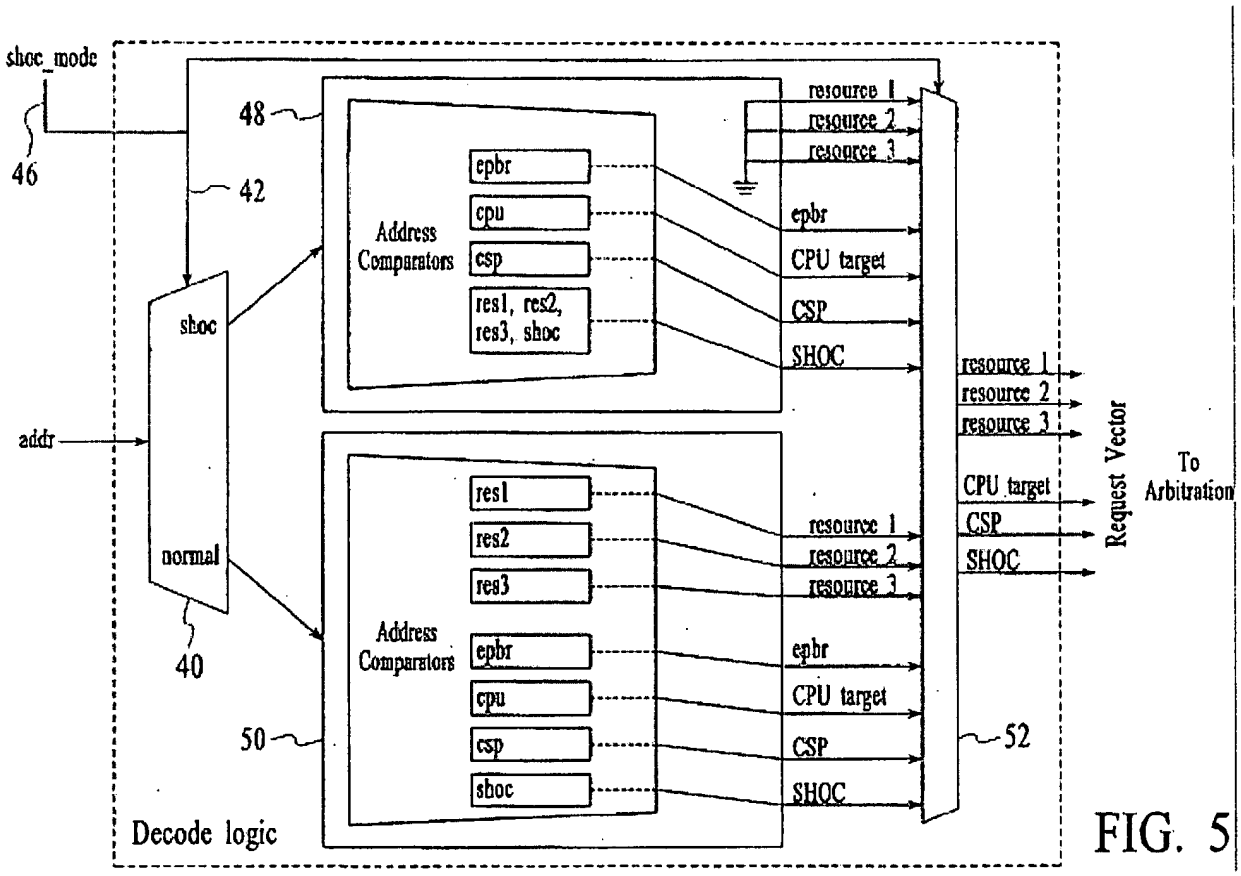


FIG. 5

Specification, Figure 5, pages 7–8.

The embodiment to which independent claim 12 is directed includes the same features described above in connection with independent claim 1, as well as off-chip circuit 32 including off-

chip external memory resources 34. Specification, Figure 1.

The embodiment to which independent claim 20 is directed is a method or process of operating the system described above in connection with independent claim 1.

The embodiment to which independent claim 26 is directed includes the same features described above in connection with independent claim 1, except for the decode logic.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1–6, 8–9, 12–17 and 26 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Mitsuishi*.

ARGUMENT

The rejection of claims 1–6, 8–9, 12–17 and 26 under 35 U.S.C. § 102(e).

Stated Grounds of Rejection:

Claims 1–6, 8–9, 12–17 and 26 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Mitsuishi*.

Legal Standard:

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-76 (8th ed. rev. 5 August 2006).

Claims 1–6, 8–9, 12–17 and 26:

Independent claims 1, 12 and 26 all recite an interface and first and second address maps, where the first address map allocates a first range of addresses to an on-chip resource and a second range of addresses to an off-chip interface while the second address map allocates the first range of addresses to the off-chip interface. That is, the first range of addresses map to an on-chip resource in the *first address map* while that same first range of addresses map to the interface in the *second address map*; *only* the second range of addresses map to the interface in the *first address map*. By way of further example, the specification describes a platform mode in which the address space includes a first portion allocated to memory resources 16, 18, etc. and a second portion allocated to the SHOC interface 20/EMI 16, as well as a bond-out mode in which the entire address space –

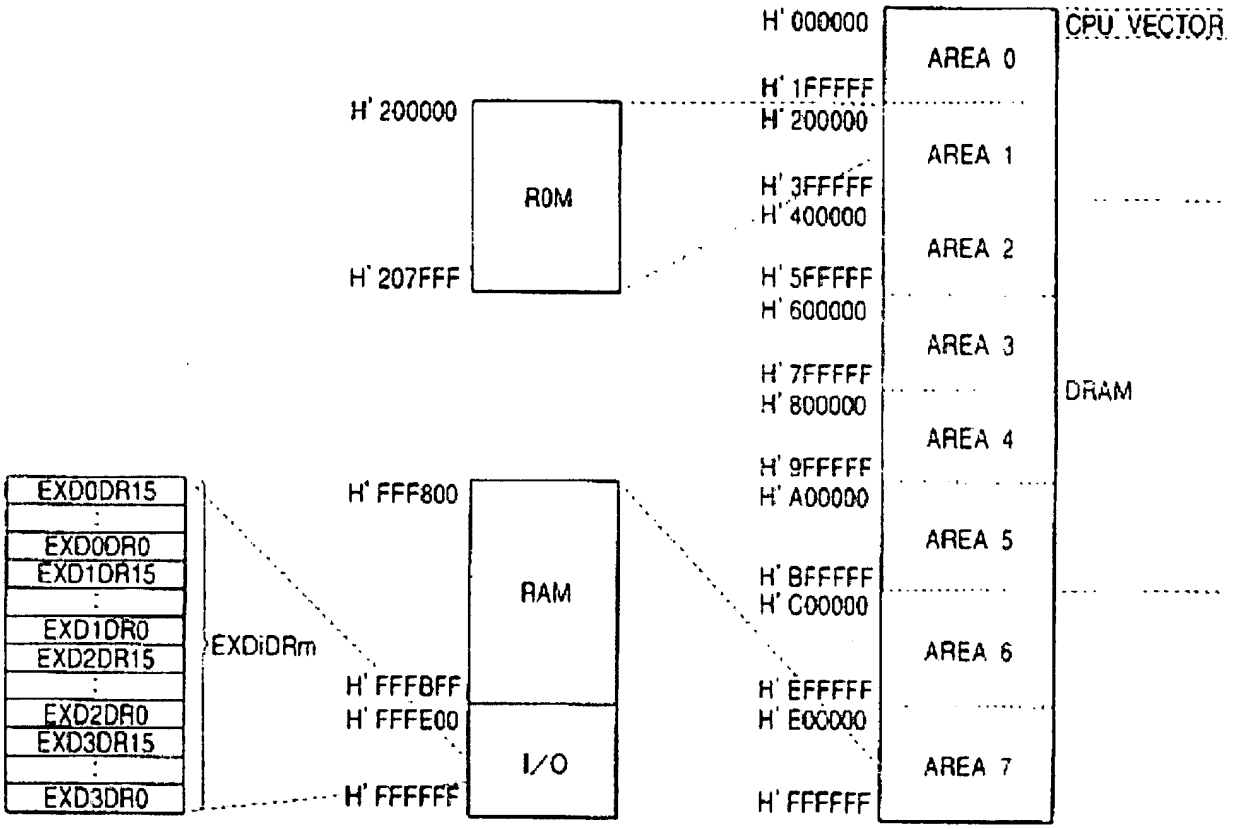
including the first portion as well as the second portion – is allocated to the SHOC interface 20. Specification, pages 5–6. According to the specification:

> This allows two prototyping modes to be used depending on the nature of the system being developed, while utilizing the same evaluation chip 2. Platform mode allows a customer to preserve the address map of the evaluation chip 1, and integrate their IP only into the memory space occupied by the SHOC port while bond-out mode allows the user to decide to use the evaluation chip 2 only as a CPU core, using the entire memory space for their own IP.

Specification, page 6.

Such a feature is not found in the cited reference. First, contrary to the assertion in the Office Action, Figure 2 of *Mitsuishi* does NOT show two different address maps as asserted in the Office Action. Instead, Figure 2 illustrates only a single address map for the addresses within the range H' 000000 through H' FFFFFF that have been logically divided into a number of areas AREA 0 through AREA 7. In Figure 2 of *Mitsuishi*, the addresses ranges allocated to ROM, RAM and I/O are depicted together with the specific addresses within the I/O range that are allocated to particular data-transfer channel buffer registers:

FIG. 2



Mitsuishi, Figure 2. Only a single mapping of the address range H' 000000 through H' FFFFFF is depicted in Figure 2 (with the address mappings depicted in greater detail and specificity as one moves toward the left), not two different mappings for those addresses.

Second, *Mitsuishi* does not disclose allocating one range of addresses to an *interface* in a first mode and allocating another range of addresses to that same *interface* in a second mode. The cited portion of *Mitsuishi* merely teaches allocating different addresses ranges to a *memory* (ROM 5) in

different modes:

> The ROM 5 has a typical size of 32 kbyte which is mapped onto addresses H' 200000 to H' 207FFF.
>
> . . . .
>
> By setting a proper operating mode, the address range allocated to the embedded ROM 5 can be changed to area 0 . . .

Mitsuishi, column 14, lines 7–8 and column 15, lines 20–21. That is, either a first address range (H' 000000 through H' 007FFF within AREA 0) or a second address range (H' 200000 through H' 207FFF within AREA 1) is allocated to ROM 5 depending on operating mode, but *Mitsuishi* does not teach that first and second address ranges are allocated to the I/O ports in different modes

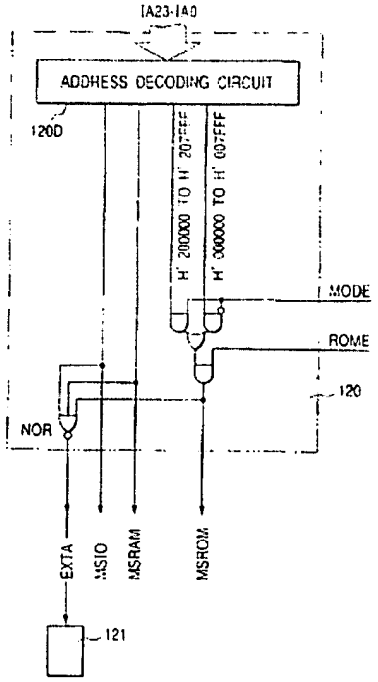
Finally, *Mitsuishi* does not teach or suggest a single address range that is mapped to an on-chip resource in one mode and to an interface in a second mode. Instead, as noted above, *Mitsuishi* merely teaches that different address ranges – either a first address range (H' 000000 through H' 007FFF within AREA 0) or a second address range (H' 200000 through H' 207FFF within AREA 1) *in the same address map* – can be allocated to ROM 5 to allow for use of a processor (CPU) without an external ROM. *Mitsuishi*, column 14, lines 7–8 and column 15, lines 20–21. *Mitsuishi* does not teach that either of the two address ranges can be allocated first to ROM 5 in one mode and then to input/output (I/O) ports 21–26, 31–35 in a second mode.

Claims 2 and 13:

Claims 2 and 13 each recite a mode setting pin employed to selectively utilize either the first address map or the second address map. In an exemplary embodiment, shoc_mode pin 46 controls

which address map 48, 50 is employed. Specification, Figure 5, page 7. Such a feature is not found in the cited reference. The "MODE" signal in Figure 4 of *Mitsuishi* is not utilized to select one of two address maps, but is instead merely logically combined with selected address bits to selectively enable (or not enable) a particular memory device MSROM:

FIG. 4



Mitsuishi, Figure 4. Note that the cited portion of *Mitsuishi* reads:

> FIG. 4 is a block diagram showing a typical address decoding circuit 120D included in the internal-bus controller 120. The address decoding circuit 120D decodes an address output by the CPU 2 or the DMAC 3 to the internal address bus IAB to recognize which of the ROM 5, the RAM 6, the I/O means 70 or a component in the external space is used as an accessed target. *An MSROM signal, an MSRAM signal, an MSIO signal or an EXTA signal is activated as a select signal obtained as*

> *a result of address decoding to indicate that the ROM 5, the RAM 6, the I/O means 70 or a component in the external space respectively is recognized as an accessed target.*
>
> As described earlier, the ROM 5 can be mapped onto area 0 or 1 of the address map shown in FIG. 2 in dependence on the operating mode of the microcomputer 1. The ROM 5 can also be put in an unusable state by resetting a ROME signal shown in FIG. 4 at "0" through selection of a predetermined operating mode or specification of an internal I/O register.

Mitsuishi, column 18, lines 23–40 (emphasis added). As apparent, MODE contributes to a device select signal, not an address map selection signal. This portion of *Mitsuishi* also reinterates that a *memory*, not an *interface*, is mapped to different areas of an address map, rather than the same area of an address map being mapped to different interfaces as recited in the claims.

Claims 3 and 14:

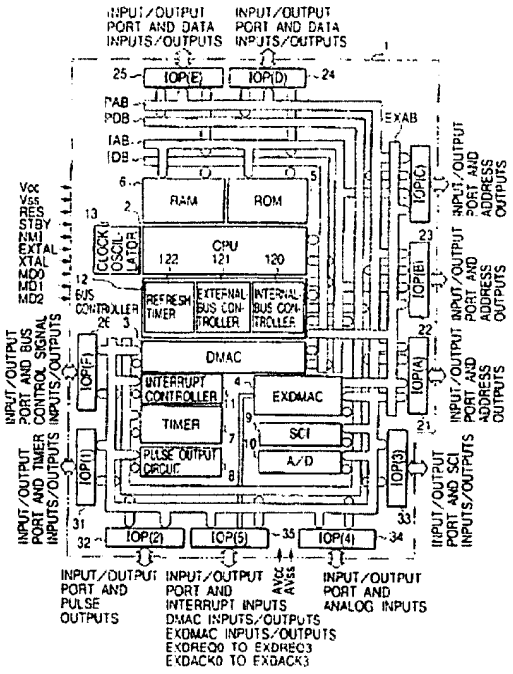
Claims 3 and 14 each recite switching circuitry responsive to the mode setting pin selectively directing memory access requests to either the first address map or the second address map. In an exemplary embodiment, multiplexer 40 controls which address map 48, 50 receives addresses for memory access requests. Such a feature is not found in the cited reference. *Mistuishi* discloses no switching circuitry for switching between first and second address maps, either in general or specifically in response to the MODE signal. Contrary to the assertion in the Office Action, the logic gates in Figure 4 of *Mitsuishi* do NOT form a multiplexer, but instead are simple logic gates for generate a device enable signal.

Claims 9 and 17:

Claims 9 and 17 each recite a chip-side port for transmitting memory access requests in

parallel and first and second circuit-side ports each with a reduced number of pins for communication memory access request packets off-chip. Such a feature is not found in the cited reference. The cited portion of *Mitsuishi* does not disclose that any of input/output ports 21–26 or 31–35 have sufficient pins for parallel transmission of memory access request packets on the chip (processor) side by have a reduced number of pins on the circuit (off-chip) side:

FIG. 1



Mitsuishi, Figure 1.

REQUESTED RELIEF

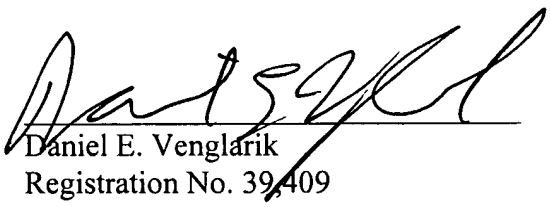
The Board is respectfully requested to reverse the outstanding rejections and return this application to the Examiner for allowance.

The Commissioner is hereby authorized to charge any fees connected with this communication (including any extension of time fees) or credit any overpayment to Munck Butrus Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS, P.C.

Date: 1-26-2007



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APPENDIX A
CLAIMS APPENDIX

1. (Original) An integrated circuit comprising:

a processor operable to issue memory access requests, each memory access request identifying an address in memory to which the request is directed;

at least one on-chip resource falling within the address space addressable by the processor;

an interface for directing packets off-chip and addressable within the address space of the processor; and

a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps,

wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in said second memory address map said first range of addresses are also allocated to the interface.

2. (Previously Presented) An integrated circuit according to claim 1, which comprises a mode setting pin for selectively setting a first mode in which said first address map is utilized and a second mode in which said second address map is utilized.

3. (Original) An integrated circuit according to claim 1, wherein said request directing unit comprises switching means responsive to a mode setting signal for selectively directing the memory access request to one of said first and second address maps.

4. (Original) An integrated circuit according to claim 3, wherein said switching means comprises a multiplexer.

5. (Original) An integrated circuit according to claim 1, wherein said at least one on-chip resource comprises a memory mapped peripheral.

6. (Original) An integrated circuit according to claim 1, wherein said at least one on-chip resource comprises a memory access device connectable to an off-chip memory resource.

7. (Original) An integrated circuit according to claim 1, which comprises control registers addressable in said memory space, wherein in said first memory address map said first range of addresses include addresses of control registers associated with said at least one resource and in said second address map said addresses are reallocated to control registers associated with the interface.

8. (Original) An integrated circuit according to claim 2, wherein said mode is set by application of a logic value selected from one and zero on the mode setting pin.

9. (Original) An integrated circuit according to claim 1, wherein said interface comprises at least one chip-side port for transmitting memory access requests in parallel across a plurality of pins, and first and second circuit-side ports each with a reduced number of pins for communicating said packets off-chip.

10. (Original) An integrated circuit according to claim 9, wherein said interface comprises circuitry for chopping a packet transmitted on the chip-side port into chunks so as to be transmitted in a plurality of cycles on the reduced number of pins on the first circuit-side port.

11. (Original) An integrated circuit according to claim 10, wherein the interface further comprises circuitry for reassembling chunks received in a plurality of cycles on said set of pins at said second circuit-side port into a single packet for transmission via said at least one chip-side port.

12. (Original) A prototype system comprising an integrated circuit comprising:

a processor operable to issue memory access requests, each memory access request identifying an address in memory to which the request is directed;

at least one on-chip resource falling within the address space addressable by the processor;

an interface for directing packets off-chip and addressable within the address space of the, processor;

a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps, wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in the second memory address map said first range of addresses are also allocated to the interface; and

an off-chip circuit connected to said interface and including at least one off-chip memory resource.

13. (Previously Presented) A prototype system according to claim 12, which comprises a mode setting pin operatively connected to the request directing unit for selectively setting a first mode in which said first address map is utilized and a second mode in which said second address map is utilized.

14. (Original) A prototype system according to claim 12, wherein said request directing unit comprises switching circuitry responsive to a mode setting signal for selectively directing the memory access request to one of said first and second address maps.

15. (Original) A prototype system according to claim 12, wherein said at least one on-chip resource comprises a memory mapped peripheral.

16. (Original) A prototype system according to claim 12, wherein said at least one on-chip resource comprises a memory access device connectable to an off-chip memory resource.

17. (Original) A prototype system according to claim 12, wherein said interface comprises at least one chip-side port for transmitting memory access requests in parallel across a plurality of pins and first and second circuit-side ports each with a reduced number of pins for communicating said packets off-chip.

18. (Original) A prototype system according to claim 17, wherein said interface comprises circuitry for chopping a packet transmitted on the chip-side port into chunks so as to be transmitted in a plurality of cycles on the reduced number of pins on the first circuit-side port.

19. (Original) A prototype system according to claim 12, wherein the interface further comprises circuitry for reassembling chunks received in a plurality of cycles on said set of pins at said second circuit-side port into a single packet for transmission via said at least one chip-side port.

20. (Original) A method of evaluating a prototype system comprising an integrated circuit including an on-chip processor associated with at least one on-chip memory resource and an off-chip circuit associated with at least one off-chip memory resource, the method comprising:

executing a computer program on the on-chip processor, said program causing the generation of memory access requests, each memory access request including an address identifying an address in memory to which the request is directed; and

in accordance with a selected mode of operation, selectively supplying said memory access requests to at least one of said first and second memory address maps, and directing the memory access requests selectively to said on-chip memory resource or said off-chip circuit in dependence on the selected one of said first and second address maps.

21. (Original) A method according to claim 20, wherein said mode of operation is selected by application of selectable logic values to a mode setting pin.

22. (Original) A method according to claim 20, wherein said memory access requests are directed off-chip via an interface whose address space replaces the address space of the on-chip memory resource in the second memory address map.

23. (Original) A method according to claim 22, wherein said memory access requests take the form of packets.

24. (Original) A method according to claim 23, wherein packets are chopped into chunks and transmitted in a plurality of cycles when being conveyed off-chip.

25. (Original) A method according to claim 23, wherein chunks received in a plurality of cycles from the off-chip circuit are reassembled into packets for transmission on-chip.

26. (Original) An integrated circuit comprising: processing means operable to issue memory access requests, each memory access request identifying an address in memory to which the request is directed; at least one on-chip resource falling within the address space addressable by the processing means; interface means for directing packets off-chip and addressable within the address space of the processing means; and means for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps, wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface and in the second address map the first range of addresses are also allocated to the interface.

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APPENDIX B
EVIDENCE APPENDIX

None.

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APPENDIX C
RELATED PROCEEDINGS APPENDIX

None.